

Verilog 作業

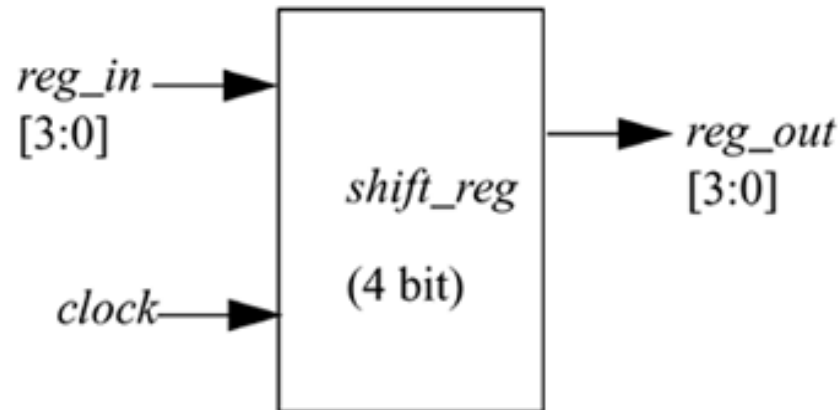
ch4 : Exercise 4.3 , Exercise 4.4

ch5 : Exercise 5.4

ch6 : Exercise 6.3

CH4 Exercises

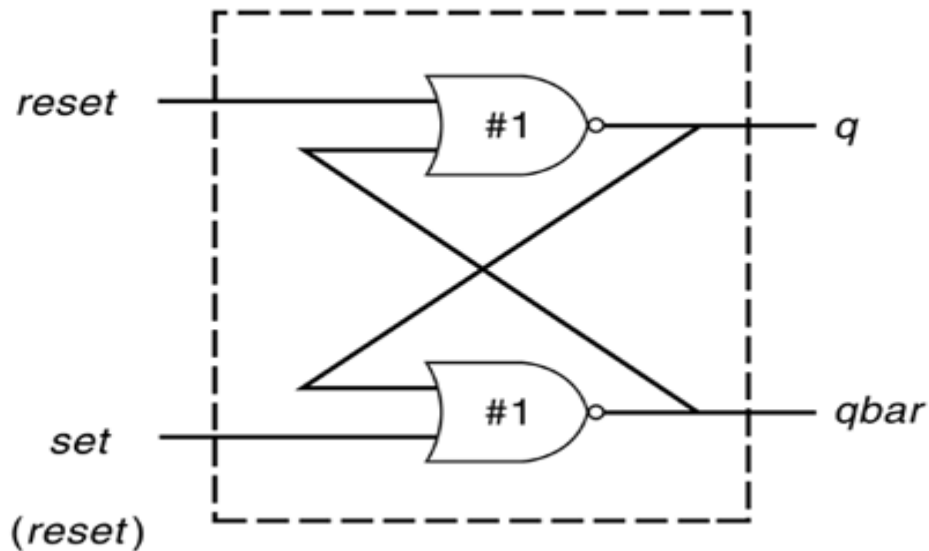
- 1. (Exercise 4.3): A 4-bit parallel shift register has I/O pins as shown in the figure below. Write the module definition for this module `shift_reg`. Include the list of ports and port declarations. You do not need to show the internals.



-
- **2.(Exercise4.4)**: Declare a top-level module stimulus. Define REG_IN (4 bit) and CLK (1 bit) as reg register variables and REG_OUT (4 bit) as wire. Instantiate the module shift_reg and call it sr1. Connect the ports by ordered list.
-

CH5 Exercises

- 1. (Exercise 5.4): The logic diagram for an RS latch with delay is shown below. Write the Verilog description for the RS latch. Include delays of 1 unit when instantiating the nor gates. Write the stimulus module for the RS latch, using the following table, and verify the outputs.



set	reset	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	?

CH6 Exercises

-
- **1.(Exercise6.3):** A synchronous counter can be designed by using master-slave JK flipflops. Design a 4-bit synchronous counter. Circuit diagrams for the synchronous counter and the JK flipflop are given below. The clear signal is active low. Data gets latched on the positive edge of clock, and the output of the flipflop appears on the negative edge of clock. Counting is disabled when count_enable signal is low. Write the dataflow description for the synchronous counter. Write a stimulus file that exercises clear and count_enable. Display the output count Q[3:0].
-

Figure 6-5. Master-Slave JK-flipflop

